REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

Several editorial amendments have been made to place the specification and abstract in better form.

Non-elected Claims 1-10 have been cancelled, while Claims 25-32 have been newly presented in order to provide more comprehensive protection for certain aspects of Applicants' invention. Accordingly, Claims 11-32 are pending. It should be noted that the cancellation of Claims 1-10 is intended solely to avoid the payment of additional fees in connection with new Claims 25-32 and, as such, is without prejudice to Applicants' right to present the cancelled claims in a continuing application.

Turning to the merits, Claims 11-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hashimoto et al. (Hashimoto). Without acceding to the rejection, each of independent Claims 11 and 19 has been amended to better define the invention intended to be claimed. More particularly, Claim 11 has been amended to clarify that the etching prevention film is formed on a sidewall portion of the first insulating film, but so as not to cover sidewall portions of the first gate electrode. See, for example,

etching prevention film 17 in Fig. 21 of the subject application. Analogously, independent Claim 19 has been amended to recite that the etching prevention film is formed on both sidewall portions of the patterned first protection insulating film but so as not to cover sidewall portions of the floating gate electrode and control gate electrode formed in the step (d). New independent Claim 26 includes a similar limitation. By so forming the etching prevention film, Applicants' invention allows for removal of damaged gate oxide film adjacent to the gate electrode while at the same time avoiding a reduction in width of the protective insulating film covering the gate electrode. Indeed, in a preferred form addressed in newly presented dependent Claims 25, 31, and 32, the first gate insulating film may be processed such that it retreats beneath opposite sidewall portions of the gate electrode. See gate oxide film 6 in Fig. 28.

It is apparent that the aforementioned features of Applicants' invention distinguish patentably from the cited teachings of Hashimoto. Note in particular that the silicon nitride sidewall spacers 55' in Figs. 39(a) and 39(b) cover the full height of the gate electrode sidewalls

and thus cannot be equated with the etching prevention film of Applicants' invention as now claimed.

Accordingly, it is respectfully requested that the rejection on Hashimoto be withdrawn and that this application be passed to issue.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§1.16 and 1.17 which may be required by this paper, and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, then such extension is hereby requested.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:sjk

Miles & Stockbridge P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102
(702) 903-9000

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Marked-up Copy of the Abstract:

ABSTRACT OF THE DISCLOSURE

[Promoting mass storage and a fine structure of each flash memory.]

An insulating film for protecting an upper portion of a control gate electrode is constituted by a silicon oxide film, and thereby stress affecting a gate oxide film and a substrate that is located below a bottom portion thereof is reduced. Further, an etching prevention film consisting of a silicon nitride film is formed on a sidewall of the silicon oxide film, and thereby it is possible to prevent the sidewall of the silicon oxide film from being etched in a hydrofluoric acid cleaning step after processing of a gate electrode.

Marked-up Copy of the Paragraphs:

Page 7:

Please substitute the following paragraph for the paragraph beginning at line 10:

Due to this, as shown in FIG. 50, when a silicon nitride film 108 serving as a sidewall insulating film is deposited on the semiconductor substrate 100 in the next step, stepped portions are generated on the silicon nitride film 108 in the vicinity of respective boundaries between each control gate electrode 104 and the silicon [nitride] oxide film 105. As a result, when contact holes are formed in the space regions of the gate electrodes (floating gate electrodes 102 and control gate electrodes 104) by means of the SAC technique, the silicon nitride film 108 on each stepped portion described above is removed and thickness thereof becomes thin. Thereafter, a problem of defects has occurred such that a metal film embedded into each contact hole and the control gate electrode 104 become closer to each other in the vicinity of each stepped portion described above, and both become short-circuit according to circumstances. The problem like this arises even in the case where the protection insulating film covering the

upper portion of each control gate electrode 104 is formed of a laminating film consisting of a silicon oxide film and a silicon nitride film.

Page 8:

Please substitute the following paragraph for the paragraph beginning at line 2:

As stated above, by consideration of the [inventions] inventors, it has become clear that if a part of or all of the protection insulating film covering the upper portion of each control gate electrode is formed of a silicon oxide film in order to suppress stress of the gate oxide film and the substrate of the lower portion thereof, the stress being resulted from the silicon nitride film, then it is extremely difficult to realize the micro-fabrication of the MISFET by utilizing the SAC technique.

Marked-up Copy of the Claims:

11. (Amended) A method for manufacturing a semiconductor integrated circuit device including a MIS transistor structure, the method comprising the steps of:

(a) forming a first gate insulating film for forming the MIS transistor structure on a main surface of a semiconductor substrate;

(b) forming at least one pair of laminating structure bodies each including two layers of a first gate electrode covering a part of said first gate insulating film and a first insulating film covering said first gate electrode, an etching prevention film being formed on a sidewall portion of said first insulating film but so as not to cover sidewall portions of said first gate electrode;

(c) introducing impurities into said semiconductor substrate through said first gate insulating film located in a region [uncovered] not covered with said laminating structure bodies, and thereby forming a first impurity introduced region self-aligned with said laminating structure bodies on the main surface of said semiconductor substrate[.];

(d) removing said first gate insulating film in the region [uncovered] not covered with said laminating structure bodies after said step (c); and

(e) forming a second insulating film covering upper portions and sidewall portions of said laminating structure bodies after said step (d).

19. (Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming, on a main surface of a semiconductor substrate, a first gate insulating film consisting of a silicon oxide film, and forming a first conductive film, a second gate insulating film and a second conductive film over said first gate insulating film in this order:

(b) forming a first protection insulating film consisting of [one of] a single layer [film and a laminating film, said single layer film being a] silicon oxide film formed over said second conductive film, [and said] with or without a laminating [film being a] silicon nitride film formed over the silicon oxide film;

(c) patterning said first protection insulating film, and thereby forming an etching mask consisting of said first protection insulating film;

(d) patterning said second conductive film, said second gate insulating film and said first conductive film in this order by dry etching using said etching mask as a mask, and thereby forming a plurality of gate electrodes that each have a floating gate electrode [consisting] formed by a portion of said first conductive film and a control gate electrode [consisting] formed by a portion of said second conductive film and that each have a laminating structure in which an upper portion of said control gate electrode is covered with said first protection insulating film;

(e) forming an etching prevention film consisting of a silicon nitride film on [both sidewall portions of said] the patterned first protection insulating film [patterned], after said step (c) and before said step (d), or after said step (d), said etching prevention film being formed on both sidewall portions of the patterned first protection insulating film but so as not to cover sidewall portions of said floating gate electrode and said control gate electrode formed in said step (d);

(f) introducing impurities into the main surface of said semiconductor substrate located between sidewall portions facing each other in said plurality of gate electrodes, and thereby forming a source region and a drain region;

(g) treating a surface of said semiconductor substrate by using etchant containing a hydrofluoric acid after said step (f), and thereby cleaning said first gate insulating film located between the sidewall portions which face each other in said plurality of gate [insulating film] electrodes;

(h) covering an upper portion and both sidewall portions of each of said plurality of gate electrodes after said step (g), and forming a second protection insulating film consisting of a silicon nitride film having such a thickness as to partially embed a region between the sidewall portions which face each other in said plurality of gate electrodes;

(i) forming, on an upper portion of said second protection insulating film, an interlayer insulating film consisting of a silicon oxide film, and embedding, with said interlayer insulating film, the region between the

sidewall portions which face each other in said plurality of gate electrodes;

(j) etching said interlayer insulating film and said second protection insulating film located between the sidewall portions which face each other in said plurality of gate electrodes, and thereby forming a first connection hole for exposing a surface of said source region and a second connection hole for exposing a surface of said drain region; and

(k) forming a third conductive film electrically connected to said source region inside said first connection hole, and forming a fourth conductive film electrically connected to said drain region inside said second connection hole.

21. (Amended) The method for manufacturing a semiconductor integrated circuit device according to claim 20,

wherein each of said plurality of gate electrodes constitutes [a] part of a respective memory cell of a flash memory, and writing into said memory cell is carried out by injecting a charge into said floating gate electrode thereof, and erasing from said memory cell is carried out

by discharging, to said semiconductor substrate, said charge injected into said floating gate electrode thereof.